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Hardware Design of 2 Dimensional Discrete Wavelet Transform By using VLSI

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Abstract - Discrete Wavelet Transform brings their own strong benefits to that environment a local outlook, a multiscaled outlook, cooperation between scales, and a time-scale analysis. DWT performs multi-resolution analysis which enables to have a scale-invariant interpretation of image. Because of superior energy compaction and correspondence with human visual system, two-dimensional DWT (2D-DWT) has been proven to be a key operation in image processing.

To optimize speed and memory requirement, we propose novel VLSI architecture for 2D DWT using Conditional Carry Adder [3].This work discusses architecture, working and implementation of multiplier less 1D DWT and 2D DWT in detail using 5/3 & 9/7 filter. Performance results of 1D and 2D DWT using Xilinx are presented.

Key words - Discrete wavelet transform (DWT), 5/3& 9/7 filter, Conditional Carry Adder, Xilinx & Synplify.

1. INTRODUCTION

THIS paper represents an approach towards VLSI implementation of the 2-dimentional Discrete Wavelet Transform (DWT).In this paper the DWT is implemented by using 5/3 filter coefficients. This led us to choose multiplier less architecture using 5/3 or 9/7 filter banks for DWT implementation.

Over the past several years, the wavelet transform has gained widespread acceptance as an indispensable tool in many applications like computer graphics, telecommunication, numerical analysis, signal processing especially valued with audio/video signal processing. Many times a particular spectral component occurring at any instant can be of particular interest.In these cases it may be beneficial to know the time intervals these particular spectral components occur.Wavelet transform helps to carry out such studies.

Discrete Wavelet Transform (DWT), a type of wavelet transform, brings their own strong benefits to that environment: a local outlook, a multiscaled outlook, cooperation between scales, and a time-scale analysis [1]. This makes wavelet good choice for verity of applications.DWT based schemes have outperformed other coding schemes like the ones based on Discrete Cosine Transform (DCT). One of the prominent applications of it is Federal Bureau of Investigation (FBI) fingerprint compression.

DWT performs multi-resolution analysis (MRA) of a signal with localization in both time and frequency. Multi-resolution decomposition enables to have a scale invariant interpretation of image[1].Because of superior energy compaction and correspondence with human visual system, two-dimensional DWT (2D-DWT) has been proven to be a key operation in image processing Since ASIC can offer higher processing speeds and better throughput

besides consuming less silicon area, it would be the obvious choice for implementing architecture for computationally intensive signal processing related applications.

However, it is appropriate to confirm the functionality and robustness of proposed architecture by prototyping and using re-programmable type devices (like FPGA2) before taping Graphic Data System (GDS) files for ASIC processing. Due to the availability of Xilinx programmable logic design suite it was further proposed to implement 2D DWT in suitable FPGA and carry out the extensive testing for the same.

The main subjective of this the dissertation work were:

1. To decide a suitable architecture of DWT for VLSI implementation.
2. To implementation and test 1D DWT and 2D DWT in FPGA using 5/3 & 9/7 filter.
3. To propose and test a suitable architecture for 2D DWT from memory and speed point of view.

2. PREVIOUS WORK

A lot of literature survey was carried out to understand basics of wavelet transform and its extension to DWT.

Maurizio Martina and Guido Masera proposed multiplierless architecture using the advantage of biorthogonality.Architecture is derived using vanishing moment condition, impulse response of filters are arranged in lesser multipliers and made those multipliers in two's power. Also they designed 9/7 biorthogonal wavelets using 5/3 biorthogonal wavelets.

Hazem H. Alietal. Recommended the use of mixed parallel and sequential architecture there by reducing the overall numbers of multipliers in comparison with only parallel structure[4]. The realization of db6 DWT using QMF is proposed. In this architecture multiplexer is used to select proper input along with proper multiplier coefficients.

Sang Yoon Park has presented a totally multiplier less lattice structure reducing the hardware complexity with improved stop band [5]. Distributed arithmetic approach for DWT implementation has been presented by Amit Acharyya which resulted into reduced memory requirement and power [6]. A novel architecture was proposed by Chao Cheng and Keshab K. Parhi [7] with claim to reduce the computation time. Implemented DWT based on parallel FIR structure which achieves computational time of N2/12.

3. FUNDAMENTALS OF WAVELET THEORY

Wavelet provides a time-scale representation of signals as an alternative to traditional time frequency representation. Wavelets are class of functions used to localize a given function in both time and frequency (space and scaling). They belongs to square integral functions (L2(R)) and has zero mean ($\int \varphi dt = 0$). Family of wavelet is constructed from mother and daughter wavelet. Daughter wavelets are formed by translation and dilation of mother wavelet. Wavelet can be classified as Wavelet Series Expansion, Continuous Wavelet Transform (CWT) and Discrete Wavelet Transform (DWT). The basis of CWT is represented as

$$\varphi_{a,b}(t) = \frac{1}{\sqrt{a}} \varphi\left(\frac{t-b}{a}\right) \quad \ldots\ldots\ldots\ldots\ldots (1)$$

where a is translation parameter and b is scaling parameter. Continuous Wavelet

Transform (CWT) is defined as projection of function on wavelet basis function.

$$W(a,b) = \int f(t) \frac{1}{\sqrt{a}} \varphi\left(\frac{t-b}{a}\right) dt \ldots\ldots (2)$$

3.1 Overview of DWT Algorithm

In this section Wavelet, Filter Bank and Multiresolution Signal Analysis have been traditionally used independently in the fields of applied mathematics, signal processing and computer vision, respectively, have now been converged to form a single theory known as Mallats-Herringbone algorithm. According to it, DWT can be efficiently implemented using subband coding (SBC) scheme.When talking about wavelets, we mostly mean a pair of functions: the scaling function ϕ and the wavelet function ψ

Let Vi and Wi be the space spanned by the set of basis ϕ and ψ respectively.

$\_\_\_\subset V_{-1} \subset V_0 \subset V_1 \subset \_\_\_$

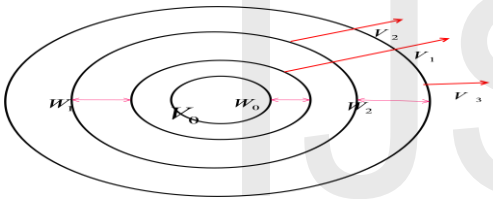

Figure1:Multi Resolution Anaiysis

i.e. any signal in V1 can be represented using the basis of V2 and so on. It means lower resolution of signal can be computed by linear combination of higher resolution signals. The self similarity (refinement condition) of the scaling function ϕ is bounded to a filter h and is defined by

$\phi(x) = \sum_n h\phi(n)\sqrt{2}\,\phi(2x-n)$ …….(3)

Biorthogonal wavelets can be constructed from B-spline wavelet basis [5]. B- spline of given order can be expressed as linear combination of scaled and translated version of itself i.e. it follows scaling relation but their integer translates, except Haar, are not orthogonal. Hence it becomes necessary to calculate its dual scaling function.

JPEG 2000 consists of two types of wavelet filter banks, namely 9/7 biorthogonal filter and 5/3 biorthogonal filter.The former has lossy compression while the later has lossless compression.The numbers indicates the number of LPF and HPF filter coefficients respectively. The low frequency components (smooth variations) constitute the base of an image, and the high frequency components (the edges which give the detail) add upon them to refine the image, thereby giving a detailed image.

A 2-D separable DWT is equivalent to two consecutive 1-D transforms. For an image, a 2-D DWT is implemented as a 1-D row transform followed by a 1-D column transform as shown in Figure 2. Transform coefficients are obtained by projecting the 2-D input image onto a set of 2-D basis functions that are expressed as the product of two 1-D basis

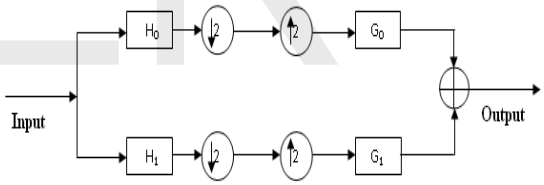

Figure 2: Analysis and Synthesis Filter Bank

4. Implementation of DWT algorithm

In the FDWT part the input data will be transferred from time domain to scale domain. Then in thresholding part some of the coefficients will be set to zero and in the IDWT part the coefficients will be transferred back into time domain.

JPEG 2000 uses 5/3 filter for lossless compression. The LPF coefficients of 5/3 filters are $\sqrt{2}$ [-1/8; 2/8; 6/8; 2/8;-1/8] and The HPF coefficients of 5/3 filters are $\sqrt{2}$ [-1/2; 1;-1/2].These can be implemented in FPGA using registers, shifters and adders and

multipliers. While implementing the algorithm 5/3 biorthogonal filter multiplierless architecture is proposed which reduces the complexity.The $\sqrt{2}$ is normalization factor. It can be taken care in hardware at either analysis/synthesis part by 1 bit shifting since data gets multiplied by $\sqrt{2}$ at analysis as well as synthesis part which is effectively multiplication by 2. The development of algorithm in VHDL is different in some aspects. The main difference is unlike MATLAB, VHDL does not support many built in functions such as convolution, mux, mod, flip flop and many more. So while implementing the algorithm in VHDL, linear equations of FDWT and IDWT [10] is used. The floating point operations have been avoided here. The VHDL code is compiled and simulated using Xilinx and Aldec Active HDL 3.5 software.

Next, the VHDL codes were synthesized using the synthesis tool "Synplify or Xilinx" which have produced "gatelevel architecture" for VLSI implementation. Finally, the design codes of DWT have been downloaded into FPGA board for verifying the functionality of the design. The simulation results shown in figure 3,4,5 & 6 and also the synthesis results are presented.The equations of 5/3 filter are given by

$W_0 = X_i$

$W_1 = X_{i-1} + X_{i+1}$

$W_2 = X_{i-2} + X_{i+2}$

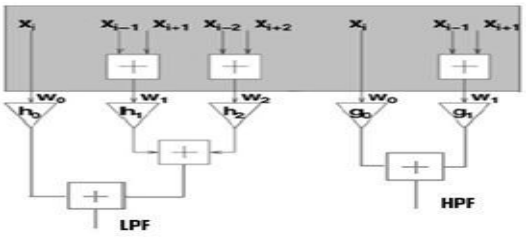

Figure 3: 5/3 Direct Implementation

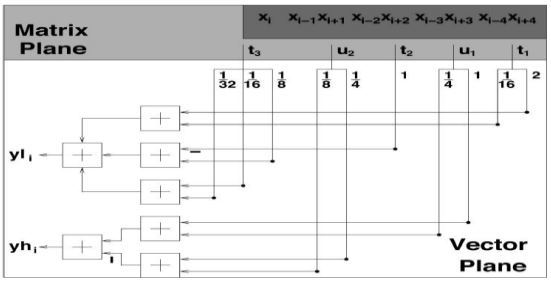

Figure 4: Fast Modified 9/7 Implementation.

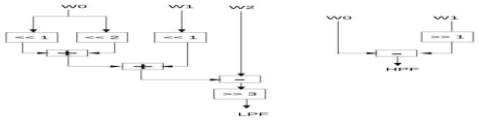

Figure 5: Modified Multiplierless 5/3 Implementation

5. REQUIRED H/W & S/W

Synthesis is performed to transform the VHDL code into logic gate level using Synplify 7.0 & VHDL using Xilinx , FPGA kit Vertex IV.

6. RESULT

The output of DWT implimented with xilinx is shown in figure 5.This work focuses on the digital VLSI implementation of DWT (FDWT and IDWT) algorithm using VHDL [10]. In order to increase the performance and reduce computational complexities many modifications have been made. A simple i/p is applied X[n].

X[n]={0,80,592,1104,848,1872,208,120,240,8,1008, 1848,1468,2040….}

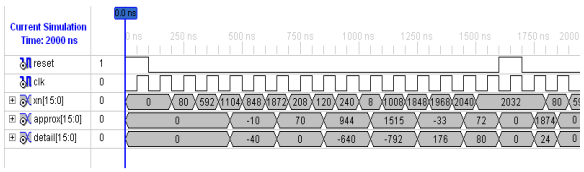

Figure 6:The output of DWT using 5/3 filter coef.

Table 8.1: Results Using MATLAB and Xilinx for Analysis 5/3 Filters

MATLAB LPF Output	MATLAB HPF Output	Xilinx LPF Output	Xilinx HPF Output
0	0	0	0
-10	-40	-10	-40
-54	-216	-54	-54
70	0	70	70
634	384	634	384
944	-640	944	-640
1280	1344	1280	1344
1515	-792	1515	-792
518	-104	518	-104
– – –	– – –	– – –	– – –

Table 8.2: Results Using MATLAB and Xilinx for Synthesis 5/3 LPF

Input	MATLAB LPF Output	Xilinx LPF Output
0	0	0
80	40	40
592	376	376
1104	1104	1104
848	1824	1824
1872	2336	2336
208	2400	2400
– – –	– – –	– – –

We have found that higher decomposition is expected to cause higher compression ratio. In order to reduce the complexity and increase computation speed, linear algebra equations of DWT are used while implementing the algorithm in VHDL.This linear algebra approach gives almost the same output.

7. CONCLUSION

1) A detail study of VLSI architecture for 1D and 2D DWT is carried out. The 5/3 and 9/7 biorthogonal wavelet which are suggested by JPEG 2000 standard are implemented without multipliers.
2) Results from FPGA shows that 5/3 biorthogonal wavelets are better than 9/7 with respect to memory utilization and speed. Truncation error is negligible for 5/3 biorthogonal wavelet. A novel architecture for 2D DWT is proposed and implemented in FPGA. The 2D DWT is tested on 8 * 8 image, results of 2D DWT are encouraging.

8. References

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